

N-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME55N06 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

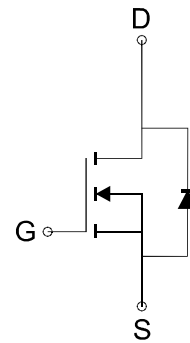
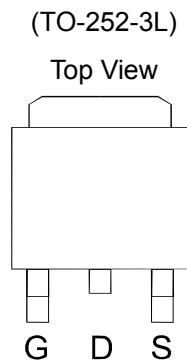
FEATURES

- $R_{DS(ON)} \leq 9.5m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME55N06 (Pb-free)

ME55N06-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	Tc=25°C	64
		Tc=70°C	51
Pulsed Drain Current	I_{DM}	256	A
Maximum Power Dissipation	P_D	Tc=25°C	63
		Tc=70°C	40
Operating Junction and Storage Temperature Range	T_J	-55 to 150	°C
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	2	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics ($T_c = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
I _{GSS}	Gate-Body Leakage	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	μA
R _{DS(ON)}	Drain-Source On-Resistance	$V_{GS}=10V, I_D=25A$		7.5	9.5	m Ω
V _{SD}	Diode Forward Voltage	$I_S=25A, V_{GS}=0V$		0.85	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	$V_{DS}=44V, V_{GS}=10V, I_D=25A$		114		nC
Q _g	Total Gate Charge	$V_{DS}=44V, V_{GS}=4.5V, I_D=25A$		23		
Q _{gs}	Gate-Source Charge			31		
Q _{gd}	Gate-Drain Charge			43		
C _{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		5030		pF
C _{oss}	Output Capacitance			597		
C _{rss}	Reverse Transfer Capacitance			194		
R _g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		0.8		Ω
t _{d(on)}	Turn-On Delay Time	$V_{DD}=28V, R_L=28\Omega, V_{GS}=10V, R_G=4.5\Omega$		43		ns
t _r	Turn-On Rise Time			25		
t _{d(off)}	Turn-Off Delay Time			105		
t _f	Turn-Off Fall Time			30		

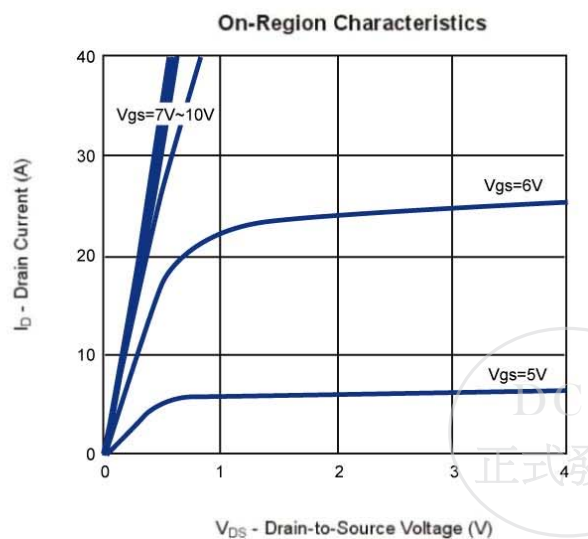
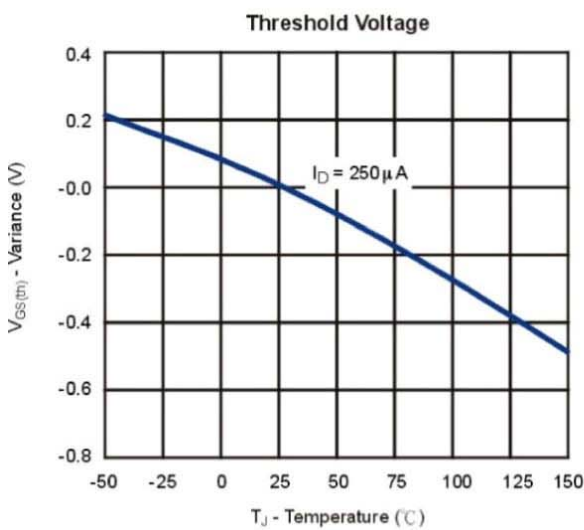
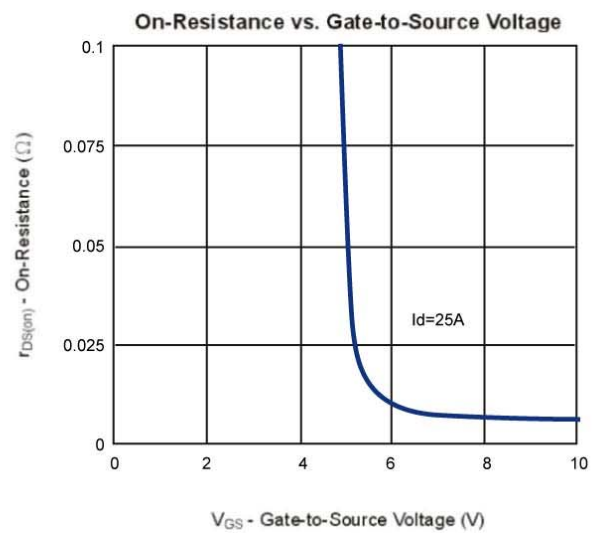
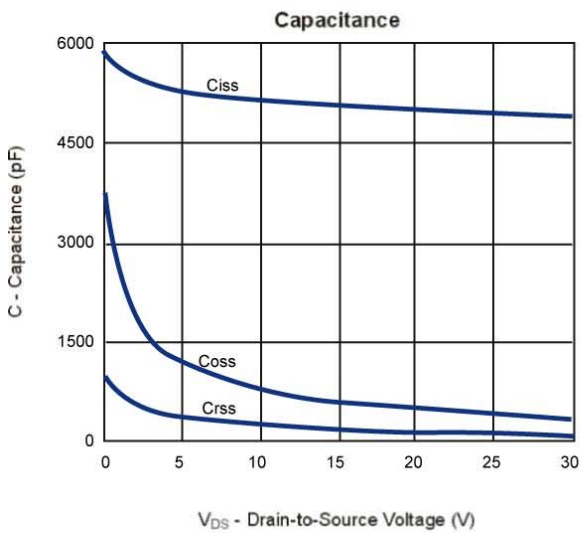
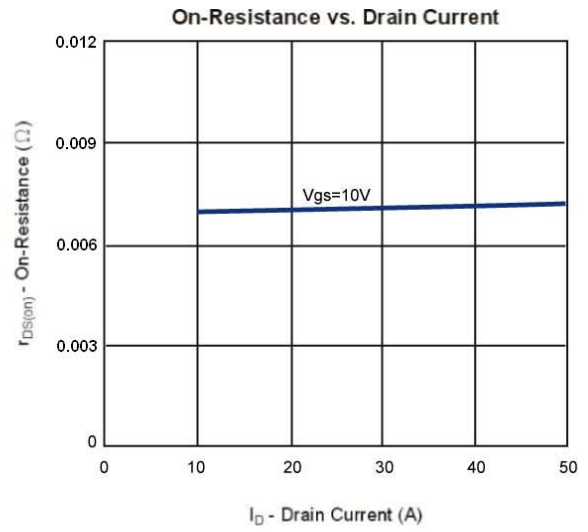
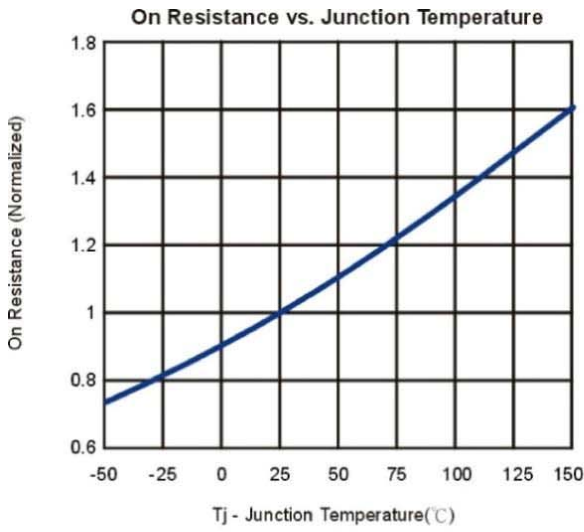
 Note: a. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



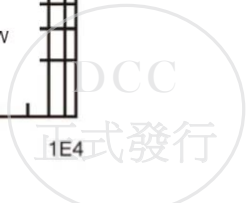
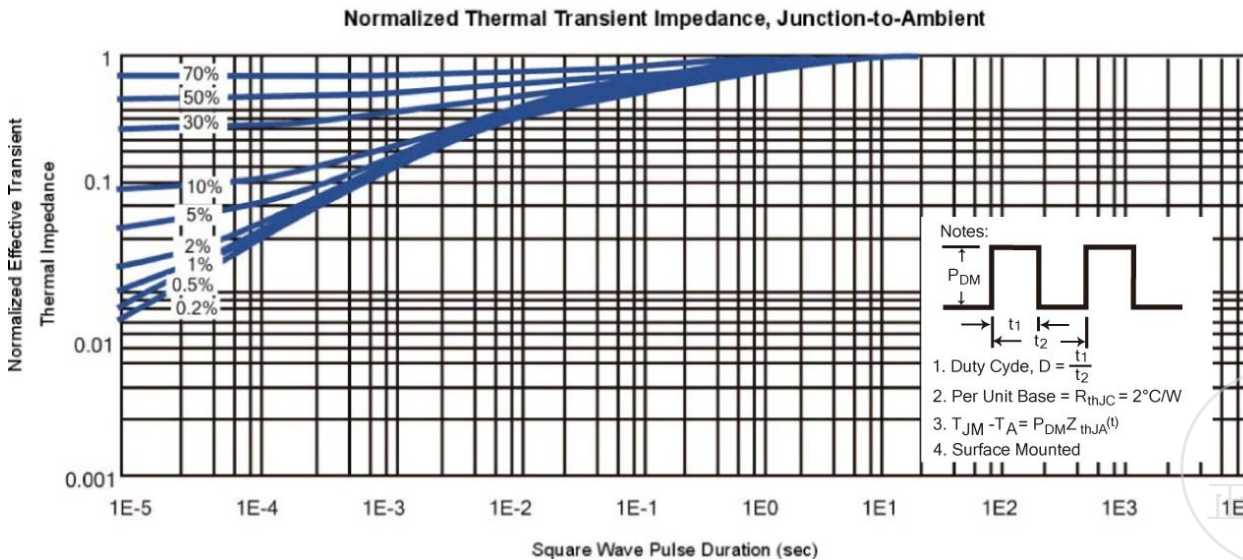
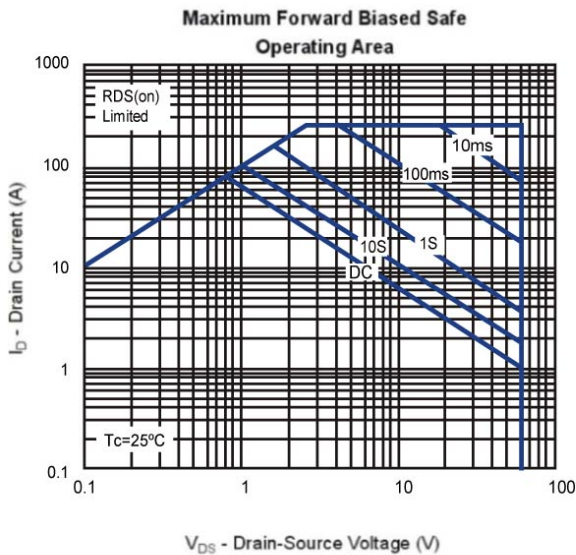
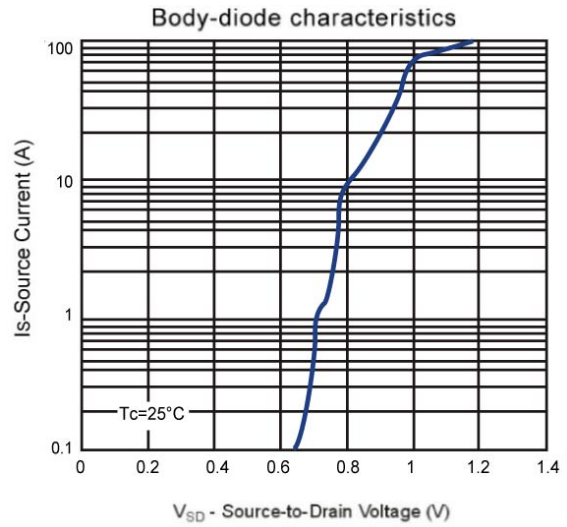
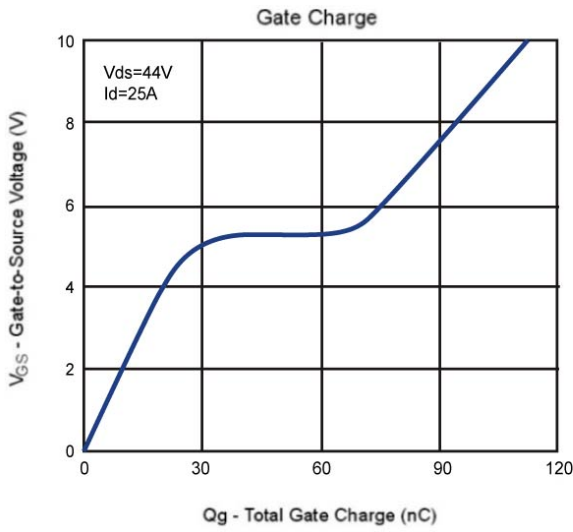
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Typical Characteristics (T_J = 25°C Noted)

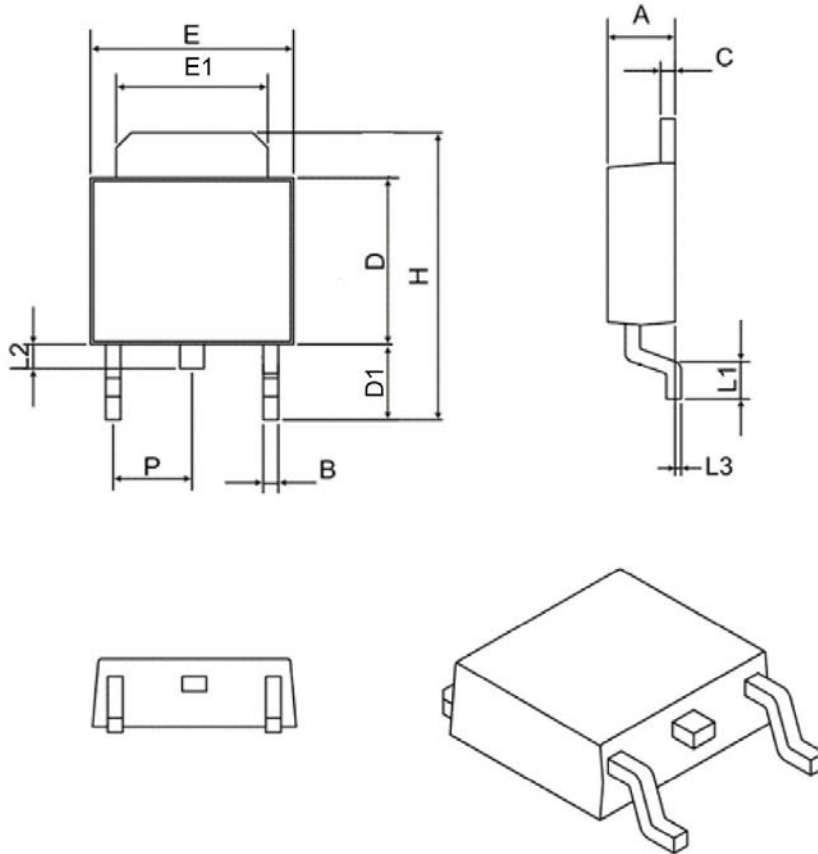


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TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

